Electronic Version
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Claims

[c1] 1.A self-biased differential buffer comprising:

a first input;

a second input;

a first current source transistor that drives a first current to a first upper branch node;

a first upper drive transistor having a gate receiving the first input, and a drain driving a first output, for conducting a first drive portion of the first current;

a first upper bias-generating transistor, having a gate receiving the first input, and a drain driving a first bias-generating node, for conducting a first bias-generating portion of the first current;

a first lower drive transistor having a gate receiving the first input, and a drain driving the first output, for conducting to a first lower branch node;

a first lower bias-generating transistor, having a gate receiving the first input, and a drain driving the first bias-generating node, for conducting to the first lower branch node;

a first current sink transistor that sinks current from the first lower branch node;

a first transmission gate between the first bias-

generating node and a bias node;

a second current source transistor that drives a second current to a second upper branch node;

a second upper drive transistor having a gate receiving the second input, and a drain driving a second output, for conducting a second drive portion of the second current;

a second upper bias-generating transistor, having a gate receiving the second input, and a drain driving a second bias-generating node, for conducting a second bias-generating portion of the second current;

a second lower drive transistor having a gate receiving the second input, and a drain driving the second output, for conducting to a second lower branch node;

a second lower bias-generating transistor, having a gate receiving the second input, and a drain driving the second bias-generating node, for conducting to the second lower branch node;

a second current sink transistor that sinks current from the second lower branch node; and

a second transmission gate between the second bias-generating node and the bias node.

[c2] 2.The self-biased differential buffer of claim 1 wherein the bias node carries a bias voltage applied to a gate of the first current source transistor and to a gate of the

second current source transistor.

[c3] 3.The self-biased differential buffer of claim 2 wherein the bias node is connected to a gate of the first current sink transistor and to a gate of the second current sink transistor.

[c4] 4.The self-biased differential buffer of claim 3 wherein the first transmission gate comprises a first p-channel transmission gate transistor and a first n-channel transmission gate transistor that conduct current in parallel between the first bias-generating node and the bias node;

wherein the second transmission gate comprises a second p-channel transmission gate transistor and a second n-channel transmission gate transistor that conduct current in parallel between the second bias-generating node and the bias node.

[c5] 5.The self-biased differential buffer of claim 4 wherein a gate of the first p-channel transmission gate transistor and a gate of the second p-channel transmission gate transistor are driven by an active-high reset signal or an active-high power-down signal that is activated by being driven to a high voltage to disable the first and second p-channel transmission gate transistors during a reset or during a power-down mode;

wherein a gate of the first n-channel transmission gate transistor and a gate of the second n-channel transmission gate transistor are driven by an active-low reset signal or an active-low power-down signal that is activated by being driven to a low voltage to disable the first and second n-channel transmission gate transistors during the reset or during the power-down mode,
whereby the first and second transmission gates are disabled during reset or the power-down mode.

[c6] 6.The self-biased differential buffer of claim 2 wherein the first drive portion of the first current is greater than the first bias-generating portion of the first current, whereby more current is used for generating outputs than for generating the bias voltage.

[c7] 7.The self-biased differential buffer of claim 6 wherein the first drive portion of the first current is ten times greater than the first bias-generating portion of the first current.

[c8] 8.The self-biased differential buffer of claim 2 further comprising:
a first upper reset transistor, connected in series to conduct the first current between the first current source transistor and the first upper branch node;
a first lower reset transistor, connected in series to con-

duct between the first lower branch node and the first current sink transistor;

a second upper reset transistor, connected in series to conduct the second current between the second current source transistor and the second upper branch node;

a second lower reset transistor, connected in series to conduct between the second lower branch node and the second current sink transistor;

wherein the first and second upper reset transistors receive a reset signal that stops current conduction through the first and second upper reset transistors during reset or during a power-down mode;

wherein the first and second lower reset transistors receive an active-low reset signal that stops current conduction through the first and second lower reset transistors during reset or during the power-down mode.

[c9] 9.The self-biased differential buffer of claim 8 wherein the first and second upper reset transistors are p-channel transistors;

wherein the first and second lower reset transistors are n-channel transistors.

[c10] 10.The self-biased differential buffer of claim 9 further comprising:

a first output buffer, having an input receiving the first output, for driving a first buffered output;

a second output buffer, having an input receiving the second output, for driving a second buffered output, whereby the first and second outputs are buffered.

[c11] 11.The self-biased differential buffer of claim 10 further comprising:
a first buffered reset transistor for driving the first output to a first state during reset or during the power-down mode;
a second buffered reset transistor for driving the second output to a second state that is a complement of the first state during reset or during the power-down mode.

[c12] 12.A balanced self-biased differential buffer comprising:
first amplifier means, receiving a first input, for generating a first output and a first bias node, the first amplifier means comprising:
first current source means for generating a first current to a first upper node in response to a self-bias node;
first current sink means for receiving a current from a first lower node in response to the self-bias node;
first upper drive transistor means for driving a current from the first upper node to the first output in response to the first input;
first upper self-bias transistor means for driving a current from the first upper node to the first bias node in response to the first input;

first lower drive transistor means for driving a current from the first output to the first lower node in response to the first input;

first lower self-bias transistor means for driving a current from the first bias node to the first lower node in response to the first input;

first transmission gate means for conducting between the first bias node and the self-bias node;

second amplifier means, receiving a second input, for generating a second output and a second bias node, the second amplifier means comprising:

second current source means for generating a second current to a second upper node in response to the self-bias node;

second current sink means for receiving a current from a second lower node in response to the self-bias node;

second upper drive transistor means for driving a current from the second upper node to the second output in response to the second input;

second upper self-bias transistor means for driving a current from the second upper node to the second bias node in response to the second input;

second lower drive transistor means for driving a current from the second output to the second lower node in response to the second input;

second lower self-bias transistor means for driving a

current from the second bias node to the second lower node in response to the second input; and
second transmission gate means for conducting between the second bias node and the self-bias node,
whereby the self-bias node is generated between the first and second transmission gate means.

[c13] 13.The balanced self-biased differential buffer of claim 12 wherein the first and second upper drive transistor means, the first and second upper self-bias transistor means, and the first and second current source means comprise p-channel transistors;
wherein the first and second lower drive transistor means, the first and second lower self-bias transistor means, and the first and second current sink means comprise n-channel transistors.

[c14] 14.The balanced self-biased differential buffer of claim 12 further comprising:
first upper reset transistor means for blocking conduction of the first current through the first current source transistor means in response to a reset signal;
first lower reset transistor means for blocking conduction of current through the first current sink means in response to an inverse of the reset signal;
second upper reset transistor means for blocking conduction of the second current through the second cur-

rent source transistor means in response to the reset signal;

second lower reset transistor means for blocking conduction of current through the second current sink means in response to the inverse of the reset signal.

[c15] 15.The balanced self-biased differential buffer of claim 14 wherein the first and second upper reset transistor means comprise p-channel transistors; and

wherein the first and second lower reset transistor means comprise n-channel transistors.

[c16] 16.The balanced self-biased differential buffer of claim 15 wherein the first transmission gate means comprises:

a first p-channel transistor having a gate driven by the reset signal, having a channel between the first bias node and the self-bias node;

an first n-channel transistor having a gate driven by the reset signal, having a channel between the first bias node and the self-bias node;

wherein the second transmission gate means comprises:

a second p-channel transistor having a gate driven by the reset signal, having a channel between the second bias node and the self-bias node;

an second n-channel transistor having a gate driven by the reset signal, having a channel between the second bias node and the self-bias node.

[c17] 17.A self-biasing differential buffer comprising:

a first input signal;

a second input signal;

a first current-source transistor, having a gate driven by a self-bias node;

a first upper reset transistor, having a gate driven by a mode signal;

wherein the first current-source transistor and the first upper reset transistor have channels in series between a power supply and a first upper branching node;

a first upper drive transistor, having a gate receiving the first input signal, a source connected to the first upper branching node, and a drain connected to a first output node;

a first upper bias-generating transistor, having a gate receiving the first input signal, a source connected to the first upper branching node, and a drain connected to a first bias-generating node;

a first lower drive transistor, having a gate receiving the first input signal, a source connected to the first lower branching node, and a drain connected to the first output node;

a first lower bias-generating transistor, having a gate receiving the first input signal, a source connected to the first lower branching node, and a drain connected to the

first bias-generating node;
a first current-sink transistor, having a gate driven by the self-bias node;
a first lower reset transistor, having a gate driven by an inverse of the mode signal;
wherein the first current-sink transistor and the first lower reset transistor have channels in series between a first lower branching node and a ground;
a first p-channel transmission gate transistor having a gate driven by the mode signal, and a channel between the first bias-generating node and the self-bias node;
a first n-channel transmission gate transistor having a gate driven by the inverse of the mode signal, and a channel between the first bias-generating node and the self-bias node;
a second current-source transistor, having a gate driven by the self-bias node;
a second upper reset transistor, having a gate driven by the mode signal;
wherein the second current-source transistor and the second upper reset transistor have channels in series between the power supply and a second upper branching node;
a second upper drive transistor, having a gate receiving the second input signal, a source connected to the second upper branching node, and a drain connected to a

second output node;

a second upper bias-generating transistor, having a gate receiving the second input signal, a source connected to the second upper branching node, and a drain connected to a second bias-generating node;

a second lower drive transistor, having a gate receiving the second input signal, a source connected to the second lower branching node, and a drain connected to the second output node;

a second lower bias-generating transistor, having a gate receiving the second input signal, a source connected to the second lower branching node, and a drain connected to the second bias-generating node;

a second current-sink transistor, having a gate driven by the self-bias node;

a second lower reset transistor, having a gate driven by the inverse of the mode signal;

wherein the second current-sink transistor and the second lower reset transistor have channels in series between a second lower branching node and the ground;

a second p-channel transmission gate transistor having a gate driven by the mode signal, and a channel between the second bias-generating node and the self-bias node;

a second n-channel transmission gate transistor having a gate driven by the inverse of the mode signal, and a channel between the second bias-generating node and

the self-bias node.

[c18] 18.The self-biasing differential buffer of claim 17 wherein the first and second upper drive transistors, the first and second current-source transistors, the first and second upper reset transistors, and the first and second upper bias-generating transistors are p-channel transistors;

wherein the first and second lower drive transistors, the first and second current-sink transistors, the first and second lower reset transistors, and the first and second lower bias-generating transistors are n-channel transistors.

[c19] 19.The self-biasing differential buffer of claim 18 wherein the first input signal and the second input signal are differential signals driven to opposite states.

[c20] 20.The self-biasing differential buffer of claim 18 wherein the first input signal is a relatively constant reference voltage and wherein the second input signal is a time-varying input signal.

[c21] 21.The self-biasing differential buffer of claim 20 wherein the reference voltage is about half of a power-supply voltage of the power supply.